REMARKS

Regarding the Office Action:

Claims 30 – 38 are pending and under current examination. In the Final Office Action, the Examiner repeated the objection to the drawings; repeated the rejection of claims 30 – 36 under 35 U.S.C. § 112, second paragraph as indefinite; repeated the rejection of claims 37 and 38 under 35 U.S.C. § 112, second paragraph as indefinite; repeated the rejection of claims 30 – 36 under 35 U.S.C. § 102(e) as anticipated by Hsu, et al. (U.S. Patent No. 5,482,888); and repeated the rejection of claims 37 and 38 under 35 U.S.C. § 102(e) as anticipated by "Applicant's Prior Art (Fig. 2b)."

Applicants respectfully traverse the objection and rejections, as detailed above, for the following reasons.

Regarding the Objection to the Drawings:

The Examiner repeated the objection to the drawings under 37 C.F.R. § 1.83(a) (Final Office Action, p. 2).

Applicants submit that it is unclear whether the Examiner received the Supplemental Request for Approval of Drawing Changes, filed on July 16, 2003. Applicants representative placed several telephone calls to the Examiner, namely on November 7th, 13th, 24th, and 25th, 2003, and has not received a clear response from the Examiner after her promise to retrieve the file. Applicants therefore request that the Examiner confirm receipt of the July 16, 2003 Supplemental Request for Approval of Drawing Changes. This Request, supplementing the Request filed on June 30, 2003, clearly overcomes the Examiner's objection to the drawings, further in view of the remarks that follow.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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Applicants therefore explicitly demonstrate, in this Response, a link between each and every claim element and individual features shown in the drawings. Nevertheless, to counter the Examiner's erroneous allegation that "the drawings do not disclose these limitations" (Final Office Action, p. 5), Applicants explain the claimed features and their representation in the drawings. Each and every element of each pending claim is shown in the drawings.:

Claim 30:

The semiconductor device shown in Fig. 3K comprises a substrate (11), a device isolation insulating film (16) formed on one major surface of the substrate (11), a gate electrode (25) formed on the major surface of the substrate (11), a gate wiring layer (25) formed in the device isolation insulating film (16) and connected to the gate electrode (25), a source electrode (22) and a drain electrode (22) arranged on the major surface of the substrate (11) to face each other via the gate electrode (25), and an insulating film (24) covering bottom and side surfaces of each of the gate electrode (25) and the gate wiring layer (25).

Also, in the semiconductor device shown in Fig. 3K, the gate electrode (25), the gate wiring layer (25), the source electrode (22), and the drain electrode (22) have upper surface levels equal to or lower than an upper surface level of the device isolation insulating film (16).

As is evident from the above, every feature of claim 30 is illustrated in Fig. 3K.

Furthermore, the semiconductor device shown in Fig. 16X comprises a substrate (101), a device isolation insulating film (106) formed on one major surface of the substrate (101), a gate electrode (113) formed on the major surface of the substrate (101), a gate wiring layer (113) formed in the device isolation insulating film (106) and connected to the gate electrode (113), a source electrode (135) and a drain electrode (135) arranged on the major surface of the substrate

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HENDERSON
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1300 I Street, NW
Washington, DC 20005
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(101) to face each other via the gate electrode (113), and an insulating film (132) covering bottom and side surfaces of each of the gate electrode (113) and the gate wiring layer (113).

Also, in the semiconductor device shown in Fig. 16X, the gate electrode (113), the gate wiring layer (113), the source electrode (135), and the drain electrode (135) have upper surface levels equal to or lower than an upper surface level of the device isolation insulating film (106).

It is thus evident that every feature of claim 30 is illustrated in Fig. 16X.

In addition, the semiconductor device shown in Figs. 14O to 14R comprises a substrate (101), a device isolation insulating film (106) formed on one major surface of the substrate (101), a gate electrode (103) formed on the major surface of the substrate (101), a gate wiring layer (114) formed in the device isolation insulating film (106) and connected to the gate electrode (103), a source electrode (114) and a drain electrode (114) arranged on the major surface of the substrate (101) to face each other via the gate electrode (103), and an insulating film (110) covering bottom and side surfaces of each of the gate electrode (103) and the gate wiring layer (114).

Furthermore, Applicants' specification further explains the cross sections of Figs. 14O and 14P, as is clear from the description on page 46, line 23 to page 47, line 4. In the semiconductor device shown in Figs. 14O to 14R, the gate electrode (103), the gate wiring layer (114), the source electrode (114), and the drain electrode (114) have upper surface levels equal to or lower than an upper surface level of the device isolation insulating film (106).

As is evident from the above, every feature of claim 30 is illustrated in Figs. 14O - 14R.

Claim 31:

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The semiconductor device shown in Fig. 16X further comprises a source diffusion layer (130) and a drain diffusion layer (130) below the source electrode (135) and the drain electrode (135).

Again, every feature of claim 31 is illustrated in Fig. 16X.

Claim 32:

In the semiconductor device shown in Fig. 16X the gate electrode (113) and the gate wiring layer (113) have bottom surfaces lower than upper surfaces of the source and drain diffusion layers (130).

It is thus evident that every feature of claim 32 is illustrated in Fig. 16X.

Claim 33:

In the semiconductor device shown in Fig. 3K, the gate electrode (25), the gate wiring layer (25), and the source and drain electrodes (22) have upper surface levels equal to each other.

It is thus evident that every feature of claim 33 is illustrated in Fig. 3K.

Claim 34:

In the semiconductor device shown in Fig. 16X, the gate electrode (113) and the gate wiring layer (113) have upper surface levels lower than upper surface levels of the source and drain electrodes (135).

It is thus evident that every feature of claim 34 is illustrated in Fig. 16X.

Claim 35:

The semiconductor device shown in Fig. 5C is obtained by carrying out, in the method shown in Figs. 3A to 3K, the processes shown in Figs. 5A to 5C between the process shown in Fig. 3I and the process shown in Fig. 3J. Therefore, in the semiconductor device shown in Fig. 5C, similarly to the semiconductor device shown in Fig. 3K, the upper surfaces of the gate

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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electrode (25) and the gate wiring layer (25) have the height the same as the upper surface of the device isolation insulating film (16).

In the semiconductor device shown in Fig. 5C, the upper surfaces of the source and drain electrodes (22) are smaller in height than the upper surface of the device isolation insulating film (16). Hence, in the semiconductor device shown in Fig. 5C, the gate electrode and the gate wiring layer have upper surface levels higher than upper surface levels of the source and drain electrodes.

It is thus evident that every feature of claim 35 is illustrated in Fig. 5C.

Claim 36:

The semiconductor device shown in Figs. 14O to 14R comprises a connection wiring layer (114) connected to at least one of the source electrode (114), the drain electrode (114), the gate electrode (103), and the gate wiring layer (114).

In the semiconductor device shown in Figs. 14O to 14R, the connection wiring layer (114) has an upper surface level equal to the upper surface level of the device isolation insulating film (106). That is, in the semiconductor device shown in Figs. 14O to 14R, the connection wiring layer (114) has an upper surface level equal to or lower than the upper surface level of the device isolation insulating film (106).

It is thus evident that every feature of claim 36 is illustrated in Figs. 14O to 14R.

Claim 37:

The semiconductor device shown in Fig. 22K comprises a substrate (201), a gate wiring layer (212) formed on one major surface of the substrate (201), an insulating film (210, 211) interposed between the substrate (201) and the gate wiring layer (212) and covering a side surface of the gate wiring layer (212), a pair of thin films (204 and upper portion of 208) formed

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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on one major surface of the substrate (201) and arranged on two sides of the gate wiring layer (212), and a gate sidewall (207) formed on the pair of thin films (204, 208), covering the side surface of the gate wiring layer (212), and made of an insulator.

As is obvious from the description on page 69, line 17 to page 70, line 12, of the specification, the pair of thin films (204 and upper portion of 208) is formed by epitaxially growing a semiconductor on one major surface of the substrate (201).

It is thus evident that every feature of claim 37 is illustrated in Fig. 22K.

Claim 38:

As is obvious from the description on page 69, line 17 to page 70, line 12, of the specification, in the semiconductor device shown in Fig. 22K, a region (204) of the pair of thin films (204 and upper portion of 208) between the gate sidewall (207) and the substrate (201), a remaining region (upper portion of 208) of the pair of thin films (204 and upper portion of 208), and a surface region (lower portion of 208) of the substrate (201) in contact with the remaining region (upper portion of 208) contain a conductive impurity.

It is thus evident that every feature of claim 38 is illustrated in Fig. 22K.

Regarding the Rejection of Claims 30 – 36 under 35 U.S.C. § 112, 2nd paragraph:

Applicants refer the Examiner to exemplary portions of Applicants' specification to provide illustrative supporting descriptions of features of Applicants' claimed invention, as indicated below.

Claims 30 and 33:

The semiconductor devices defined in claims 30 and 33 are, for instance, manufactured by the following method. First, as shown in Fig. 3H, first grooves are formed on the device

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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isolation insulating film (16). Next, the first grooves are buried by the conductor, and CMP is performed. By this, as shown in Fig. 3I, the source and drain electrodes (22) are obtained.

After that, as shown in Fig. 3J, second grooves are formed on the device isolation insulating film (16). Next, a thin insulating film is formed on each of the bottom and sidewalls of the second grooves. Subsequently, the second grooves are buried by the conductor, and CMP is performed. By this, as shown in Fig. 3K, the insulating film (24), the gate electrode (25) and the gate wiring layer (25) are obtained.

As stated above, the gate electrode (25), gate wiring layer (25), source electrode (22) and drain electrode (22) are formed by burying and planarization processes. Therefore, the upper surface levels of the gate electrode (25), the gate wiring layer (25), the source electrode (22) and the drain electrode (22) have a height equal to or smaller than the upper surface level of the device isolation insulating film (16). That is, by the method stated above, a semiconductor device according to claim 30 may be obtained.

Claims 30, 31, 32 and 34:

The semiconductor devices defined in claims 30, 31, 32 and 34 are, for instance, manufactured by the following method. First, as shown in Fig. 16G, a device isolation insulating film (106) partially buried in the substrate (101) is formed, then the semiconductor (130) is epitaxially grown on the substrate (101). The upper surface of the semiconductor layer (130) is made smaller in height than the upper surface of the device isolation insulating film (106). The semiconductor layer (130) is utilized as source and drain diffusion layers.

Next, as shown in Fig. 16L, first grooves are formed. After that, as shown in Fig. 16M, a thin insulating film (132) is formed on the bottom and sidewalls of the first grooves. Then, the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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first grooves are buried by the semiconductor or conductor (113). Furthermore, the structure of Fig. 16O is obtained by carrying out CMP.

Then, as shown in Fig. 16U, the semiconductor or conductor (113) is partially removed. By this, second grooves are formed, and a gate electrode (113) and a gate wiring layer (113) are obtained.

After that, as shown in Fig. 16V, the second grooves are buried by insulator (137).

Subsequently, the layer (111) and the insulating film (131) are removed so as to form third grooves not shown in the drawings. These third grooves are buried by the conductor (135), and CMP is further performed. By this, as shown in Fig. 16W, the source and drain electrodes (135) are obtained.

As stated above, the gate electrode (25), gate wiring layer (25), source electrode (22) and drain electrode (22) are formed by burying and planarization processes. Therefore, the upper surface levels of the gate electrode (25), the gate wiring layer (25), the source electrode (22) and the drain electrode (22) will be equal to or smaller than the upper surface level of the device isolation insulating film (16) in height. That is, by the method stated above, a semiconductor device according in claim 30 may be obtained.

Also, Fig. 16W shows that the source diffusion layer (130) and the drain diffusion layer (130) are respectively located under the source electrode (135) and the drain electrode (135). That is, by the above-mentioned method, a semiconductor device according to claim 31 may be obtained

Further, Fig. 16W shows that the gate electrode (113) and the gate wiring layer (113) have bottom surfaces lower than upper surfaces of the source and drain diffusion layers (130).

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HENDERSON
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1300 I Street, NW
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202.408.4000
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That is, by the above-mentioned method, a semiconductor device according to claim 32 may be obtained.

In addition, according to Fig. 16W, the second grooves are buried by insulator (137), and thus the gate electrode (113) and the gate wiring layer (113) have upper surface levels lower than upper surface levels of the source and drain electrodes (135). That is, by the above-mentioned method, a semiconductor device according to claim 34 may be obtained.

Claim 35:

A semiconductor device such as that of claim 35 may be manufactured, for instance, by the following method. First, the structure shown in Fig. 3I is obtained by the above-mentioned method. Next, as shown in Fig. 5B, the source and drain electrodes (22) are partially removed so as to form grooves. After that, as shown in Fig. 5C, these grooves are buried by the insulator (31), and CMP is performed. Subsequently, the processes explained with reference to Figs. 3J and 3K are successively performed.

In the semiconductor device obtained by such a method, as shown in Fig. 5C, the upper surfaces of the source and drain electrodes (22) are smaller in height than the upper surface of the device isolation insulating film (16). Also, the upper surfaces of the gate electrode (25) and the gate wiring layer (25) are equal to the upper surface of the device isolation insulating film (16) in height. Therefore, in the semiconductor device obtained by the above-mentioned method, the gate electrode (25) and the gate wiring layer (25) have upper surface levels higher than upper surface levels of the source and drain electrodes (22). That is, by the above-mentioned method, a semiconductor device according to claim 35 may be obtained.

Claim 36:

FINNEGAN
HENDERSON
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1300 I Street, NW
Washington, DC 20005
202.408.4000
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The semiconductor device defined in claim 36 is manufactured, for instance, by the following method. In the method of manufacturing a semiconductor device explained with reference to Figs. 3H to 3K, a groove which corresponds to the source electrode (22), the drain electrode (22) and the connection wiring layer is formed as the first groove. The upper surface of the connection wiring layer obtained as such is equal to the upper surface of the source and gate electrodes in height, as shown in Figs. 14O and 14P, for example.

Therefore, in the semiconductor device obtained by this method, the connection wiring layer (114) is connected to at least one of the source electrode (114), the drain electrode (114), the gate electrode (103), and the gate wiring layer (114), and the connection wiring layer (114) has an upper surface level equal to or lower than the upper surface level of the device isolation insulating film (106). That is, by the above-mentioned method, a semiconductor device according to claim 36 may be obtained.

Applicants further direct the Examiner to the exemplary citations to Applicants' specification, claims and drawings, made above, demonstrating that Applicants' claims 30 – 36 comply with 35 U.S.C. §112, second paragraph. Applicants point out that

> "[t]hey can define in the claims what they regard as their invention essentially in whatever terms they choose so long as the terms are not used in ways that are contrary to accepted meanings in the art. [They] may use ... any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought." M.P.E.P. § 2173.01.

In light of the above explanation, Applicants traverse the Examiner's allegations, and respectfully remind the Examiner that

> "[s]ome latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the

FINNEGAN
HENDERSON
FARABOW
GARRETT &
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1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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examiner might desire. Examiners ... should not reject claims or insist on their own preferences if other modes of expression selected by applicants satisfy the statutory requirement." M.P.E.P. § 2173.02.

Applicants therefore respectfully deem the rejection of claims 30 – 36 overcome. Claims 30 – 36 fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants accordingly request withdrawal of the rejection.

Regarding the Rejection of Claims 37 and 38 under 35 U.S.C. § 112, 2nd paragraph:

Applicants refer the Examiner to exemplary portions of Applicants' specification to provide illustrative support for features of Applicants' claimed invention, as indicated below.

Claims 37 and 38:

Semiconductor devices according to claims 37 and 38 may be manufactured, for instance, by the following method. First, the structure shown in Fig. 22A is obtained. Next, as shown in Fig. 22B, a thin film (203) is patterned in a shape of the gate wiring layer. Then, a portion of the oxide film (202) not covered with the thin film (203) is removed.

Next, as shown in Fig. 22C, a semiconductor layer (204') is epitaxially grown on the substrate (201). Subsequently, as shown in Fig. 22D, an insulating film (205) is formed.

Then, as shown in Fig. 22E, a gate sidewall (207) made of insulator is formed. Subsequently, using this as a mask, an impurity is implanted into the semiconductor layer (204') and the surface region of substrate (201). By this, an extension (204) and source and drain diffusion regions (208) are obtained.

Next, as shown in Fig. 22F, an insulating film (209) is formed. Subsequently, as shown in Fig. 22G, the insulating film (209) is planarized by CMP. Further, as shown in Figs. 22H and 22I, the thin film (203) and the oxide film (202) are removed. This forms a groove.

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HENDERSON
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Washington, DC 20005
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Then, as shown in Fig. 22J, a gate insulating film (210) and a reaction preventing film (211) are formed on the bottom and sidewalls of the groove. Subsequently, the groove is buried by a gate electrode material film (212). Further, by performing CMP, the structure shown in Fig. 22K is obtained.

In the semiconductor device shown in Fig. 22K, the insulating films (210, 211) are interposed between the substrate (201) and the gate wiring layer (212), as well as cover side surface of the gate wiring layer (212). Also, a pair of thin films (204 and upper portion of 208) are arranged on both sides of the gate wiring layer (212), and, as stated above, said pair of thin films are formed by epitaxially growing the semiconductor on one major surface of the substrate (201). Further, the gate sidewall (207) made of insulator is formed on the thin film (204 and upper portion of 208), as well as covers the side surface of the gate wiring layer. That is, by the above-mentioned method, a semiconductor device defined in claim 37 can be obtained.

Also, in the semiconductor device shown in Fig. 22K, the region (204) of the thin films between the gate sidewall (207) and the substrate (201), the region (upper portion of 208) of the thin films, and the surface region (lower portion of 208) of the substrate (201) in contact with the region (upper portion of 208) contain a conductive impurity. That is, by the above-mentioned method, a semiconductor device in accordance with claim 38 may be obtained.

Meanwhile, claim 37 recites, "a pair of thin films formed by epitaxial[ly] growing a semiconductor." That is, claim 37 clearly recites the material of these thin films.

Also, as stated above, the thin film (204') exists inside the final product as the upper portion of the source and drain diffusion regions (208) and the extension (204).

In light of the above explanation, Applicants respectfully traverse the Examiner's allegations and direct the Examiner's attention to this explanation and to the previously-quoted

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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M.P.E.P. citations. Applicants further direct the Examiner to the exemplary citations to Applicants' specification, claims and drawings, made above, demonstrating that Applicants' claims 37 and 38 comply with 35 U.S.C. §112, second paragraph.

Applicants therefore respectfully deem the rejection of claims 37 and 38 overcome. Claims 37 and 38 also fully comply with the requirements of 35 U.S.C. § 112, second paragraph, and Applicants accordingly request withdrawal of the rejection.

Regarding the Rejection of Claims 30 – 36 under 35 U.S.C. § 102(e):

Applicants again respectfully traverse the rejection of claims 30 – 36 under 35 U.S.C. § 102(e) as anticipated by Hsu, and again note that the incorrect statutory subsection was used as a grounds for rejection. *See* Amendment of June 30, 2003, pp. 11 – 12.

In order to properly establish that Hsu anticipates Applicants' claimed invention under 35 U.S.C. § 102, each and every element of each of the claims in issue must be found, either expressly described or under principles of inherency, in that single reference. Furthermore, "[t]he identical invention must be shown in as complete detail as is contained in the ... claim." *See* M.P.E.P. § 2131, 8th Ed., Rev. 1 (Feb. 2003), p. 2100-70, quoting *Richardson v. Suzuki Motor Co.*, 868 F.2d 1126, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Regarding the 35 U.S.C. § 102(e) rejection, Hsu does not teach each and every element of Applicants' present invention as claimed.

The Examiner incorrectly alleged that Hsu's Fig. 2H teaches each and every element of Applicants' claimed invention (Office Action, p. 5). In contrast, however, Applicants note that Hsu does not disclose at least Applicants' claimed "said gate electrode, said gate wiring layer, said source electrode, and said drain electrode have upper surface levels equal to or lower than an upper surface level of said device isolation insulating film" (claim 30). It is clear from Hsu's

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
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Fig. 2H, for example, that contact electrode 60, electrode 62, and electrode 67 all have upper surface levels *above* field oxide (FOX) 54. *See* Hsu, for example, col. 5, l. 64 – col. 6, l. 60.

Thus, since Hsu does not disclose each and every element of Applicants' independent claim 30, Hsu does not anticipate Applicants' claimed invention. In addition to Hsu not anticipating the present invention, Hsu does not disclose an identical invention, let alone in as complete detail as contained in Applicants' independent claim 30. Applicants therefore submit that the Examiner has not met these essential requirements of anticipation for a proper 35 U.S.C. § 102(e) rejection.

Therefore, Applicants submit that independent claim 30 is allowable, for the reasons already argued above. In addition, dependent claims 31 – 36 are also allowable at least by virtue of their dependence from allowable base claim 30. Therefore, Applicants respectfully submit that the improper 35 U.S.C. § 102(e) rejection of claims 30 – 36 should be withdrawn.

Regarding the Rejection of Claims 37 and 38 under 35 U.S.C. § 102(e):

Applicant respectfully traverses the rejection of claims 37 and 38 under 35 U.S.C. § 102(e) as anticipated by "Applicant's Prior Art (Fig. 2b)" (Final Office Action, p. 4).

There requirements for a proper 35 U.S.C. § 102(e) rejection have already been set forth. Regarding the 35 U.S.C. § 102(e) rejection, "Applicant's Prior Art (Fig. 2b)" ("APA") does not teach each and every element of Applicants' present invention as claimed.

Applicants note that Fig. 2B does not disclose at least "a pair of thin films formed by epitaxial growing a semiconductor on one major surface of said substrate, and arranged on two sides of said gate wiring layer" (claim 37), and that the reference numeral 5 in Fig. 2B is the surface region of the substrate, and is not formed by epitaxial semiconductor growth on the substrate.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
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Thus, since APA does not disclose each and every element of Applicants' independent claim 37, APA does not anticipate Applicants' claimed invention. In addition to APA not anticipating the present invention, APA does not disclose an identical invention, let alone in as complete detail as contained in Applicants' independent claim 37. Applicants therefore submit that the Examiner has not met these essential requirements of anticipation for a proper 35 U.S.C. § 102(e) rejection.

Therefore, Applicants submit that independent claim 37 is allowable, for the reasons already argued above. In addition, dependent claim 38 is also allowable at least by virtue of its dependence from allowable base claim 37. Therefore, Applicants respectfully submit that the improper 35 U.S.C. § 102(e) rejection of claims 37 and 38 should be withdrawn.

Conclusion:

In making various references to the specification and drawings set forth herein, it is understood that Applicants are in no way intending to limit the scope of the claims to the exemplary embodiments described in the specification, illustrated in the drawings, and the extensive discussion supplied herein by Applicants showing support in the drawings for claim features to demonstrate full compliance with 35 U.S.C. § 112, second paragraph, and 37 C.F.R. § 1.83(b). Rather, Applicants expressly affirm that they are entitled to have the claims interpreted broadly, to the maximum extent permitted by statute, regulation, and applicable case law. Applicants respectfully point out to the Examiner that "[e]ach claim must be separately analyzed and given its broadest reasonable interpretation in light of and consistent with the written description." M.P.E.P. § 2163(II)(A)(1), p. 2100-163.

In view of the foregoing remarks, Applicants request the Examiner's reconsideration of the application and submit that the objections and rejections detailed above should be withdrawn.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

This Request should allow for immediate and favorable action by the Examiner. Applicants submit that pending claims 30 – 38 are in condition for allowance, and request a favorable action.

Should the Examiner continue to dispute the patentability of the claims after consideration of this Request, Applicants encourage the Examiner to contact Applicants' undersigned representative by telephone to discuss any remaining issues or to resolve any misunderstandings. Applicants' undersigned representative would welcome the opportunity to discuss the merits of the present invention with the Examiner if telephone communication will aid in advancing prosecution of the present application.

Please grant any extensions of time under 37 C.F.R. § 1.136 required in entering this response. If there are any fees due under 37 C.F.R. § 1.16 or 1.17, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: January 28, 2004

By: _____
David M. Longo
Reg. No. 53,235

/direct telephone: (202) 408-4489/

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com